Amendments to the Drawings:

The attached sheet of drawings includes changes to Fig. 1. This sheet, replaces the original sheet. In Figure 1, the previously omitted feature has been added.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes

REMARKS

Applicant respectfully requests reconsideration in view of the foregoing amendments and following remarks.

I. CLAIM STATUS

Claims 65-85 were pending. Claim 77 has been canceled. Claims 78 and 80 have been amended. Claims 65-76 and 78-85 remain pending.

The amendments to claims 78 and 80 are made solely to place these claims in independent form. The claim scopes are unchanged.

II. DRAWING OBJECTIONS

The examiner objected to the drawings as failing to show every feature recited in the claims. Applicant submits herewith a replacement drawing sheet in compliance with 37 CFR 1.121(d) showing the omitted feature. Paragraph 35 is also amended to comport with the amended drawing. The amendments to Fig. 1 and paragraph 35 reflect originally filed paragraph 39, which states "According to the preferred embodiment of the present invention, multiple OCLAs 125 may be provided on-chip." Accordingly, no new matter is added by these amendments.

III. REJECTIONS UNDER 35 USC § 102

Claims 77, 80-82, and 84 stand rejected under 35 USC § 102(e) as being anticipated by U.S. Pat. 6,633,838 ("Arimilli"). Claim 77 has been canceled. Applicant respectfully traverses the remaining rejections at least because the cited art fails to teach or suggest each of the claim limitations.

For example, independent claim 80 recites "wherein the word recognizers each comprise a Boolean logic section and a counter/timer section." The examiner cites Arimilli's teaching of condition select logic 150 as a trigger word recognizer, and cites Arimilli's teaching of trace data control logic 130 as a storage word recognizer. Arimilli teaches that the trace data control logic 130 generates triggers as shown in Fig. 4. *See* Arimilli c4ℓ33-39 ("The multi-state logic analyzer 120 is preferably comprised of trace data control logic 130 for generating triggers and controlling ... trace array 140"). Arimilli teaches that the condition select logic 150 operates on triggers from the trace data control logic 130 as show in Figs. 5-6. *See* Arimilli c5ℓ29-32 ("[T]he condition select logic 150

determines whether a plurality of programmable conditions have been satisfied by at least one trigger event generated by the trace data control logic 130").

Having cited the condition select logic 150 and the traced data control logic 130 as **separate** word recognizers, the examiner in rejecting claim 80 treats Figs. 4-6 as a **single** word recognizer to meet the claim limitations for each individual word recognizer. Arimilli fails to teach or suggest a trigger word recognizer and a storage word recognizer each having a Boolean logic section and a counter/timer section.

Claim 80 further recites that "the Boolean logic section includes multiple hardware match logical units that ... [each] produce an output signal that ... connects to both an AND term and an OR term, and a user selects whether the AND term or the OR term is enabled for each of the hardware match logical units." The examiner does not cite, nor can applicant find, any such teaching or suggestion in Arimilli. For at least these reasons, independent claim 80 and its dependent claims 81-82 and 84 are allowable over the cited art.

IV. REJECTIONS UNDER 35 USC § 103

Claims 65-73, 75, and 78-79 stand rejected under 35 USC § 103(a) as being unpatentable over Arimilli in view of "Applicant's Admitted Prior Art" (hereafter, "Application Paragraph 9"), and further in view of *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960). Applicant hereby traverses the remaining rejections at least because the cited art fails to teach or suggest each of the claim limitations.

Applicant first wishes to address the issue of Application Paragraph 9. Any inference that Application Paragraph 9 suggests the use of multiple on-chip logic analyzers for a single chip is an error. Applicant did not intend to teach or suggest the existence of such systems, let alone that such systems would be prior art. Applicant's remark in the background description ("In this approach, history buffers, and even on-chip logic analyzers (OCLA) are provided to acquire and store event and/or time sequenced data on the chip itself.") is poorly phrased. The intent was to acknowledge the existence of different *types* of buffers and on-chip logic analyzers that have *individually* been used alone to acquire data on the

chip itself. Applicant has amended Application Paragraph 9 to state this original intention more precisely.

Independent claim 65 recites "An integrated circuit fabricated on a chip, comprising: multiple on-chip logic analyzers." The examiner acknowledges that Arimilli fails to teach multiple on-chip logic analyzers, and cites Application Paragraph 9 and In re Harza. As noted above, Application Paragraph 9 has been amended to correct any erroneous implication that the prior art teaches multiple on-chip logic analyzers. To the contrary, multiple on-chip logic analyzers have not been found in the prior art because, as noted in the background, memory buffers and word recognizers typically associated with logic analyzers demand undesirably large amounts of chip space, representing an opportunity cost to device functionality and/or performance. It is only through the inventor's efforts in this application and an incorporated co-pending application that the presence of multiple on-chip logic analyzers even becomes practicable. As discussed in paragraph 13, the disclosed word recognizer can be implemented with a minimum of logic, providing a great deal of flexibility while consuming a relatively small amount of chip space.

The examiner cites *In re Hazra* for its statement that "mere duplication of parts has no patentable significance unless a new and unexpected result is produced." However, as explained above, it is not feasible (and therefore not obvious) to merely duplicate prior art on-chip logic analyzers. That is, without benefit of the present disclosure, one of ordinary skill in the art would not find the motivation to duplicate prior art on-chip logic analyzers and would not have a reasonable expectation of success for a chip implementation with multiple on-chip logic analyzers. The claimed invention consequently produces a new and unexpected result. For at least this reason, applicant maintains that independent claim 65 and its dependent claims 66-73 and 75 are allowable over the cited art.

As amended, independent claim 78 recites "An integrated circuit fabricated on a chip, comprising: ... multiple on-chip logic analyzers each comprising a trigger word recognizer and a storage word recognizer." For the reasons discussed above, the cited art fails to teach or suggest multiple on-chip logic

analyzers fabricated on a chip. For at least these reasons, independent claim 78 and its dependent claim 79 are allowable over the cited art.

V. ALLOWABLE SUBJECT MATTER

Claims 74, 76, 83, and 85 are objected to as being dependent on a rejected base claim. Applicant acknowledges this indication of allowable subject matter, but wishes to defer amendment of these claims pending the prosecution outcome of the base claims.

VI. CONCLUSION

In the course of the foregoing discussions, Applicant may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicant respectfully requests reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 CFR § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,

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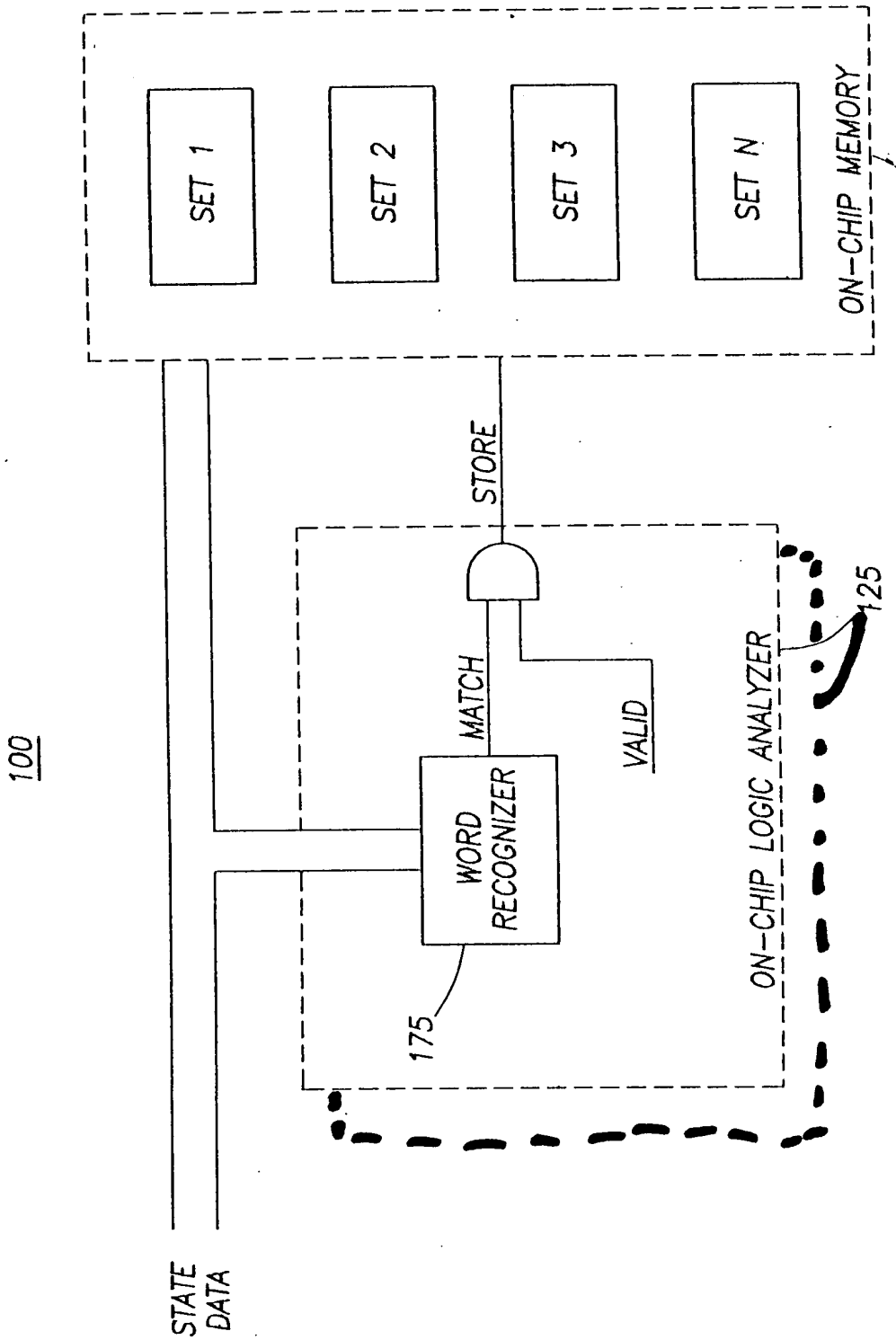
SET 1
SET 2
SET 3
SET N
ON-CHIP MEMORY
150
STORE
MATCH
VALID
WORD RECOGNIZER
175
ON-CHIP LOGIC ANALYZER
125
100
STATE DATA

FIG. 1